# Refine Search

#### Search Results -

| Terms  | Documents |
|--|-----------|
| (bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj l cell) | 12        |

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L1

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DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

L1

(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj 1

12

L1

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cell)

# Refine Search

#### Search Results -

| Terms  | Documents |
|--|-----------|
| (bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj 1 cell) | 3         |

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L2

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Clear
Interrupt

## Search History

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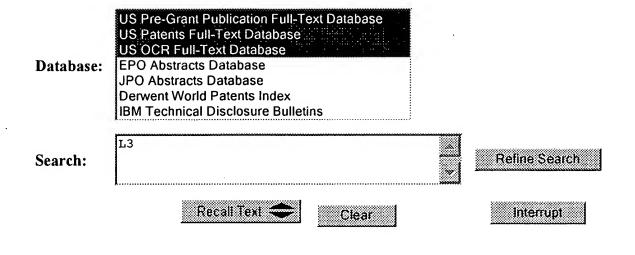
| Set<br>Name<br>side by<br>side | Query  | Hit<br>Count | <u>Set</u><br><u>Name</u><br>result set |
|--------------------------------|--|--------------|---|
| DB=E                           | PAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR  |              |   |
| <u>L2</u>                      | (bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj l cell) | 3            | <u>L2</u>                               |
| DB=P                           | GPB,USPT,USOC; PLUR=YES; OP=OR   |              |   |
| <u>L1</u>                      | (bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj l cell) | 12           | <u>L1</u>                               |

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#### Search Results -

| Terms  | Documents |
|--|-----------|
| (439/68  716/16  716/17  710/100  710/300  710/8  710/72  710/305  712/11  712/14  712/18  326/38  326/39  326/41).ccls. | 9135      |



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| Set Name side by side | Query   | Hit<br>Count | <u>Set</u><br><u>Name</u><br>result set |
|-----------------------|---|--------------|---|
| DB=P                  | GPB,USPT,USOC; PLUR=YES; OP=OR  |              |   |
| <u>L3</u>             | 710/100,300,8,72,305;712/11,14,18;716/16,17;326/38,39,41;439/68.ccls.               | 9135         | <u>L3</u>                               |
| DB=E                  | CPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR  |              |   |
| <u>L2</u>             | (bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell) | 3            | <u>L2</u>                               |
| DB=P                  | GPB,USPT,USOC; PLUR=YES; OP=OR  |              |   |
| <u>L1</u>             | (bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell) | 12           | <u>L1</u>                               |

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| Your search matched 3 of 1293212 docu<br>A maximum of 100 results are displayed, |                     | Relevance in Descending on   | der.   |                             | <b>⊠</b> e-mail | parties triend |
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| IEEE JNL IEEE Journal or Magazine  |                     |  |  |                             |                 |                |
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| ISEE CNF IEEE Conference Proceeding  | ng                  |  |  |                             |                 |                |
| IEE CONF   | ,                   | Data-driven array processor<br>Schmidt, U.; Caesar, K.; Him  |  | essing                      |                 |                |
| IEEE Standard  | •                   | Consumer Electronics, IEEE<br>Volume 36, Issue 3, Aug 19<br>Digital Object Identifier 10.11  | Transactions on<br>190 Page(s):327 - 333     |                             |                 |                |
|  |                     | AbstractPlus   Full Text: PDF  | (616 KB) KHEE ↓NI.                           |                             |                 |                |
|  | 2.                  | Programmable logic machi<br>Skokan, Z.E.;<br>Solid-State Circuits, IEEE Jo<br>Volume 18, Issue 5, Oct 19<br>AbstractPlus   Full Text: PDE                        | urnal of<br>83 Page(s):572 - 578             | ·Il array)                  |                 |                |
|  | <b></b>             | Low power mixed signal m<br>Mouine, J.;<br>Electronics Letters<br>Volume 36, Issue 23, 9 Nov<br>Digital Object Identifier 10.10<br>AbstractPlus   Full Text: PDF | r. 2000 Page(s):1913 - 19<br>149/el:20001346 | ammable cell powered urinar | y incontinen    | ce stimulator  |

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35 MO333 SEARCH

Programmable logic machine (A programmable cell array)

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Skokan, Z.E.

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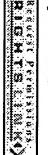
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Abstract

differs from conventional gate arrays. resulting in low cost and a four-day turnaround. This paper describes why the PLM was developed, its operational characteristics, and how it achieves subnanosecond cell delay and 400-gate complexity with less than 1 W of power, and it is fabricated through a low-density process The PLM is a single mask, programmable cell array with complete interconnect. It is 100% wireable and 100% testable with built-in LSSD, it

index Terms

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scale integration. integration bipotacintegrated.circuits cellular.arrays integrated.circuit.technology integrated.logic.circuits large Bipolar integrated circuits Cellular arrays Integrated circuit technology Integrated logic circuits Large scale

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